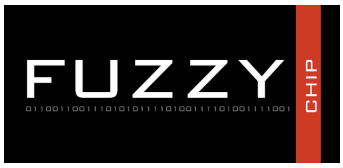

Fuzzy Chip Investment Proposal (short)

Development of Hardware MVL Technology

Executive Summary This is a brief presentation of our proposal for development of a new breed of microelectronic devices expressly designed to achieve dramatic improvements in the performance of next-generation mobile computing devices.

Our proposal

- represents a unique early investment opportunity, with a minimal downside, and a huge potential upside
- is based on proprietary disruptive next-generation technology (current-mode multivalued logic, or “MVL”) for commercial application in the fastest growing global market for semiconductor products worldwide
- involves secured IP that includes patented best-in-class MVL logic gates and applications for “blocking” patents for SoC components designed to control entry into the mobile computing market from the MVL paradigm
- offers dramatically higher computational performance, circumventing impending physical and economic limitations on the extension of Moore’s law, using existing tried-and-tested CMOS fabrication techniques
- features a detailed development plan which minimizes front-end design engineering costs while maintaining world class standards for maximal ROI by exploiting sophisticated design engineering resources in Russia

Higher Potential ROI While the global market for products based on them is rapidly expanding, design engineering and software development costs of market-competitive systems-on-a-chip (‘SoCs’) have increased markedly worldwide. For example, the design engineering budget for Qualcomm’s Snapdragon SoC famously exceeded $60 million, while the typical design engineering costs for some SoCs have now soared from $20 million at the 90 nm CMOS node to as high as $100 million at 32 nm. Software and design engineering costs are the fastest growing contributions to these king-sized budgets.

- Such huge investments have nevertheless proven profitable for fabless developers such as ARM Industries (ARMv7, MPCore™), Qualcomm

(Snapdragon™), and ST-Ericsson (NovaThor™), due to the vast and rapidly growing global market for PDAs and smart phones, which already rely heavily on SoC technology

- Our fabless silicon IP business model is designed to limit and control such costs by focusing on development of complementary components designed to be integrated as IP blocks into SoCs developed by a major industrial player, assigning as much of the front end design and programming workload as possible to competitively priced design engineering and software development resources in Russia
- At the same time final design, simulation, and verification will be assigned to a leading IC design lab (such as VIRTUS in Singapore), minimizing investment risks. This approach will guarantee world class end product design and verification standards, and enable the most sophisticated software-driven project management in the later phases, while controlling front-end design and development costs for ASIC and SoC IP

In the near term, our strategy of designing ARMv7-compatible SoC cores such as the proposed ternary multimedia coprocessor allows us to "piggyback" our complementary product on ARM's world-standard MPCore™ architecture within the ARM ecosystem, while also having the advantage that much of the investment in development of the proposed ARM-compatible multimedia coprocessor can be recycled as proven portable silicon IP into future projects for additional coprocessor cores, such as a generic high-speed floating point coprocessor, or a dedicated ultra-high speed encryption processor with extremely high inherent radiation resistance (that could be useful in military applications).

The Technology Fuzzy Chip is specifically concerned with the commercial development of a family of innovative microelectronic devices, identified by its Russian acronym as 'UMIS', and commercially exploitable systems based on it. The UMIS is a generic current mode logic gate, derived from the MSHUT, that can directly implement multivalued logic (MVL), certain variants of fuzzy logic (FL), and base-k numeric processing at hardware level, with high operational stability, exceptional reliability, a small area footprint, and minimal power requirements. The UMIS features *active internal noise suppression* and highly effective *input feedback loops* to ensure very high signal-to-noise ratios and extreme operational stability under real world conditions.

Using traditional binary hardware it's not clear how Moore's Law can be extended into the future due to physical limitations of existing lithographic and fabrication technology. Implementing MVL and base-k numeric processing *directly in hardware* can allow effective circumvention of these limits on Moore's Law while remaining squarely within the tried-and-tested CMOS fabrication paradigm. This is due to dramatically increased effective computational densities (as opposed to raw transistor counts) at the projected binary vs. MVL gate counts for fabrication scales of 32 nm, 28 nm, and beyond.

Previous MVL devices have not achieved the levels of stability and reliability needed in order to make the adoption of hardware-level MVL commercially viable. However, due to its exceptional best-in-class performance, combined with its unique feature of active internal noise suppression, Dr. Olexenko's UMIS device promises to bring this next-generation technology to full commercial realization.

Fuzzy Chip IP Portfolio The issued US and EU Olexenko patents for the generic UMIS device have been valued by JessWorld Consultancy in Singapore at $20 million. A second patent application, for a ternary inverter, has been filed in Russia by Dr. Olexenko, and a US application for the same device has been prepared and filed by IP specialists Knobbe & Martens in San Francisco. Dr. Olexenko's second patent implements a ternary inverter that can be used as a basic logic cell for ternary ASICs. Additional IP for implementations of higher level MVLs (k = 9, 27,…) will be added later for even greater performance enhancements for future development.

An additional patent application has been filed and assigned to Fuzzy Chip for a family of ARMv7-compatible ternary and higher MVL multimedia coprocessors. Such a "blocking" patent could potentially set a world standard for the design of hybrid binary-MVL coprocessors with external ARMv7 compatibility, and control access to the vast and rapidly growing market for smartphones and tablets from the MVL domain.

Collaborative Development Strategy Our proposed strategy for developing commercially marketable products based on Dr. Olexenko's UMIS device comprises the following basic steps:

- Build up Fuzzy Chip's IP portfolio with additional patents for ternary and higher level MVL devices for ultrafast numeric processing, and proposed designs for ARMv7 SoC-integrable IP based on those implementations
- Organize and equip highly qualified and exceptionally capable technologists working in Russian to perform preliminary design engineering and software development tasks, exploiting the best available project management, EDA tools, and software development methodologies
- Identify and engage a suitable IC/SoC design lab to provide best available facilities for design and verification of UMIS-based MVL ASICs in 32 and 28 nm CMOS and beyond
- Identify and engage a qualified Industrial Partner for development of commercially viable MVL ASICs, either as standalone products, or as components that can be directly integrated into industry standard architecture SoCs
- Design, independently simulate and verify, and then prototype benchmark UMIS-based MVL ASICs in selected application areas, in collaboration with the designated IC/SoC engineering design resource

- In collaboration with an Industrial Partner, bring the resulting products to market

The Company Fuzzy Chip, Pte. Ltd. is a privately held limited liability company established in Singapore in early 2011. Its officers and principals are Martti Vallila (CEO), Dr. Viktor Olexenko (Head of R&D), Eric La Fosse (Singapore Representative), and Paul Zelinsky (CTO, and San Francisco Representative). Our company's primary assets are its IP**,** and its network of resources in Russia that will facilitate the development of Hardware MVL devices under Fuzzy Chip's proposed development plan.

Fuzzy Chip's IP consists of founding and follow-up patents by Dr. Olexenko, together with additional related IP developed by Zelinsky. All IP developed by Dr. Olexenko and Zelinsky is assigned to Fuzzy Chip according to existing written agreements

Fuzzy Chip's resource base consists of privileged and trusted access to resources in Vladivostok, Novosibirsk, and Tomsk.